REMARKS

Claims 18-20 are presented for examination. Claim 18 has been amended to more clearly define the claimed invention. New dependent claims 21-24 have been added to further define the claimed subject matter.

The Examiner found the title of the application to be not descriptive. A new title is requested.

In Response, the title has been amended per the Examiner's suggestion.

Claims 18-20 have been rejected under 35 U.S.C. 101 as claiming the same invention as US patent 6,649,984.

This rejection is deemed moot in view of the amendment to claim 18.

Claim 1 of the patent recites the memory circuitry including a first circuit configured for receiving a first voltage and a second circuit configured for receiving a second voltage, the second voltage being greater than the first voltage.

By contrast, claim 18, as amended, recites, among other features, memory circuitry for storing at least data to be used by said logic circuit, said memory circuitry including a first circuit configured for receiving first and second voltages a difference of which provides a first amplitude and a second circuit configured for receiving third and fourth voltages a difference of which provides a second amplitude, the second amplitude being greater than the first amplitude.

Further, claims 18-20 have been rejected under 35 U.S.C. 102(b) as being anticipated by Sun et al. (U.S. patent 5,920,779). It is noted that this patent is not listed in the Notice of References Cited.

Claim 18, as amended, recites a semiconductor integrated circuit device, comprising:

-a logic circuit including a logic transistor formed of an insulted gate type field effect transistor as a component thereof and executing a prescribed processing; and

-memory circuitry for storing at least data to be used by said logic circuit, said memory circuitry including a first circuit configured for receiving first and second voltages a difference of which provides a first amplitude and a second circuit configured for receiving third and fourth voltages a difference of which provides a second amplitude, the second amplitude being greater than the first amplitude.

The first circuit includes as a component thereof a first-type insulated gate field effect transistor having a first gate insulting film of a single-gate structure different from a stacked gate structure having two electrodes stacked with an insulating film placed in between.

The second circuit includes as a component thereof a second-type insulated gate field effect transistor having a second gate insulating film of the single-gate structure.

The second gate insulating film is thicker than the first gate insulating film.

The logic transistor has a gate insulating film with a thickness of the first gate insulating film.

Considering the reference, Sun discloses a selective oxidation method for forming transistors having gate insulating films of different thicknesses. Figs. 6A to 6C of Sun show a DRAM embedded processing circuit. Fig. 6A shows the cross sectional structure of a logic circuit transistor having a 40 angstrom thick gate insulating film; Fig. 6B shows an I/O transistor having a 75 angstrom thick gate insulating film arranged between the DRAM and the logic circuit; and Fig. 6C shows a DRAM memory cell transistor having a 100 angstrom thick gate insulating film.

The Examiner considers the FET transistor in FIG. 6A to correspond to the logic transistor. The circuit in FIG. 6B is considered to correspond to the first circuit and the circuit in FIG. 6C is considered to correspond to the second circuit.

It is noted that FIG. 6B shows an I/O circuit which is separate from the memory circuit shown in FIG. 6C, and formed in a different portion of the substrate. Therefore, the reference fails to show that the DRAM uses transistors having gate insulating films of different thicknesses.

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.,*** 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989).

As demonstrated above, Sun does not expressly disclose the claimed memory circuitry including first and second type insulated gate filed effect transistors having gate insulating films of different thicknesses.

In the event the Examiner relied upon inherency without expressly indicating such reliance, the Examiner should be aware that inherency requires certainty, not speculation. ***In re Rijckaert***, 9 F.3rd 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); ***In re King***, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986); ***W. L. Gore & Associates, Inc. v. Garlock, Inc.***, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); ***In re Oelrich***, 666 F.2d 578, 212 USPQ 323 (CCPA 1981); ***In re Wilding***, 535 F.2d 631, 190 USPQ 59 (CCPA 1976). To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be

established by probability or possibilities. ***In re Robertson***, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

It is submitted that Sun provides no reason to conclude that the DRAM contains transistors having gate insulating films of different thicknesses. Therefore, Sun neither expressly nor under the principles of inherency discloses the claimed memory structure.

Accordingly, the Examiner's rejection under 35 U.S.C. 102 is improper and should be withdrawn.

Also, claims 18-20 have been rejected under 35 U.S.C. 103 as being unpatentable over Takebuchi.

Takebuchi discloses the logic transistor, the selection transistor and the floating gate memory transistor having the different gate insulation films. The logic transistor is used for a memory circuit peripheral transistor and for a LSI circuit transistor. The selection transistor and a high voltage transistor having a high voltage applied in the peripheral circuit have the greatest gate insulating film thickness. The memory transistor has the same gate insulation film thickness as the high voltage transistor. The other peripheral circuit transistor than the high voltage transistor has the smallest gate insulating film thickness.

The Examiner admits that Takebuchi does not disclose the claimed first circuit. However, the Examiner takes the position that it would be obvious to modify "the high voltage transistor of FIG. 2A with a transistor having a gate insulating film whose thickness D is smaller than the thickness C of the memory transistor of FIG. 2B in order to improve operating speed."

Hence, the Examiner suggests replacing the high voltage transistor of Takebuchi with a transistor having a thin gate insulating film.

The Examiner's conclusion of obviousness is respectfully traversed for the following reasons.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to provide a reason why one having ordinary skill in the art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or inference in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. ***Uniroyal, Inc. v. Rudkin-Wiley***, 837 F.2d 1044, 5 USPQ 2d 1434 (Fed. Cir. 1988); ***Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.***, 776 F.d 281, 227 USPQ 657 (Fed. Cir. 1985); ***ACS Hospital Systems, Inc. v. Montefiore Hospital***, 732 F.2d 1572, 221 USPQ 929 (Fed. Cir. 1984); ***In re Sernaker***, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983).

One skilled in the art would realize that when the high voltage transistor of Takebuchi having a thick gate insulating film is replaced with a transistor having a thin gate insulating film, the thin gate insulating film would result in a dielectric break-down caused by a high voltage.

Accordingly, the modification suggested by the Examiner would render the high-voltage transistor of Takebuchi being modified unsatisfactory for operating at a high voltage.

However, it is well settled that if proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. ***In re Gordon***, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

Hence, the modification suggested by the Examiner is improper.

Moreover, the reference provides no reason for introducing a memory circuit having transistors of a different type configured for receiving different voltages. Even if Takebuchi were modified *arguendo* as suggested by the Examiner, the modification would result in a memory

circuit having transistors with the same (but reduced compared with the original transistor) thickness of the gate insulating film. Therefore, the claimed structure would not result.

Further, Takebuchi is directed to an EEPROM, and its memory transistor is not a single-gate transistor. Claim 18, as amended, requires that the transistors of the first and second circuit are of a single-gate structure.

Takebuchi does not teach or suggest an arrangement having the gate insulating films of single-gate transistors different in thickness in different circuits.

Hence, as demonstrated above, the rejection of the claims under 35 U.S.C. 103 should be withdrawn.

In view of the foregoing, and in summary, claims 18-24 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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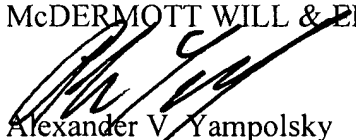

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